DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

A. Limitations as recited in the last paragraph of claim 5 include: "the second semiconductor chip is attached by adhesives and wherein the adhesives are interposed only between the second semiconductor chip and the leadframe".

However as described in the specification and Figures (see Fig. 2-6), the second chip is attached to the leadframe through the adhesives 26/29 and the molding epoxy adhesive compound (MEAC) 28, wherein the MEAC is interposed between the second chip and the leadframe as well as above the second chip.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 4-6 and 8-10, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (US Pat. Appln. Pub. 2002/0153599) in view of Kubota et al. (US Pat. 5834831).

Regarding claims 4-6 and 8-10, Chang et al. disclose a chip stacked package/CSP (20 in Fig. 2) comprising:

- a doubly down-set leadframe having a down-set tip (23 and 231 respectively in Fig. 2; para 0008) to be wire-bonded
- a first semiconductor chip (21 in Fig. 2; para 0008) attached under the down-set tip of the leadframe by a first adhesive material/ lead-on-chip tape (24 in Fig. 2; para 0009)
- first bonding/metal wires (26 in Fig. 2; para 0008) electrically connecting bonding pads of the first semiconductor chip with the down-set tip of the leadframe
- a second semiconductor chip (22 in Fig. 2; para 0008) attached on the leadframe
- second metal wires (27 in Fig. 2; para 0008) electrically connecting the second semiconductor chip with the leadframe, and
- a conventional adhesive package body (PB)/adhesive compound (AC)/epoxy molding compound/EMC (28 in Fig. 2; para 0007) sealing/encapsulatlng the first and second semiconductor chips, the first and second metal wires and a portion of the leadframe, and

- wherein the second semiconductor chip is attached to the leadframe by adhesives including a second adhesive material/a LOC tape and the PB/AC/EMC (25 and 28 respectively in Fig. 2; para 0010) wherein the adhesives are filled in the entire space between the second semiconductor chip and the first semiconductor and the second adhesive material (25 in Fig. 2; para 0010) is interposed partially only between the second semiconductor chip and the leadframe.

(Fig. 2; para 0006-0010).

Chang et al. fail to teach the backside of the first semiconductor chip being exposed.

Kubota et al. teach an encapsulated leadframe package molded in an EMC (39 in Fig. 15A) comprising:

- a backside of a semiconductor chip (see 36 in Fig. 15A; para Col. 9, lines 30-50) is exposed from the EMC to provide improved thermal dissipation being exposed epoxy, and
- a tip of a lead being wire bonded having a thickness that is less than that of a portion of the lead (see 62a and 62 in Fig. 15A) adjacent to the tip to provide reduced length of bonding wires and reduced package thickness (Col. 5, lines 5-34; Col. 9, lines 30-50).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the backside of the first semiconductor chip being

exposed or a tip that is wire bonded having a thickness that is less than that of a portion of the down-set leadframe adjacent to the tip as taught by Kubota et al. so that the thermal dissipation, the electrical performance and the reliability can be improved in Chang et al's CSP.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (US Pat. Appln. Pub. 2002/0153599) and Kubota et al. (US Pat. 5834831) as applied to claim 1 above and further in view of Smith et al. (US Pat. Appl. Pub. 2004/0065945).

Regarding claim 7, Chang et al. and Kubota et al. teach substantially the entire claimed structure as applied to claim 1 above, except the first semiconductor chip being attached under the leadframe by means of a B-stage material interposed there between.

Smith et al. teach a semiconductor chip being attached under a leadframe by a conventional B-stage adhesive material (see 42/32 in Fig. 2E; para 0050).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first semiconductor chip being attached under the leadframe by means of a B-stage material as taught by Smith et al. so that the chip bonding can be improved in Chang et al. and Kubota et al's CSP.

Response to Arguments

6. Applicant's arguments with respect to the rejected claims have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

4-19-10

/Nitin Parekh/

Primary Examiner, Art Unit 2811